(hereinafter may be simply referred to as "PCB") 48b fixed on a lower housing 48a. The PCB 48b is formed with a plurality of cartridge terminals 48c, 48c,...on its surface while arranged in a width direction. Among them, two cartridge terminals 481c and 482c located at one end of the PCB 48b in the width direction are connected with each other, and composes a switch SW1.

On the other hand, the cartridge connector 46 is formed with an oblong inserting portion 46a to insert therein the tip end portions of the lower housing 48a and the PCB 48b, and a plurality of connector terminals 46b, 46b,... being arranged in the width direction are formed inside the inserting portion 46a. As can be understood from Figure 5, each connector terminal 46b is brought into close contact with an upper housing 46c at a proper location of a longitudinal direction, and fixed there. The connector terminal 46b bends from the upper housing 46c to the inserting portion 46a, and bends toward the upper housing 46c again. A plurality of rectangular shaped openings through each of which one end of each connector terminal 46b is exposed are formed above the inserting portion 46a and arranged in the width direction.

A metallic piece is provided so as to cross over two openings at a proper location in the center of the width direction, and composes a switch SW2. Two connector terminals 463b and 464b being exposed through the two openings are electrically connected by the switch SW2 when no external force is applied.

If the tip end portions of the lower housing 48a and the PCB 48b are inserted into the inserting portion 46a, each connector terminal 46b is raised by the lower housing 48a and the PCB 48b and brought into contact with the each cartridge terminal 48c on the PCB 48b. Connector terminals 481a and 481b are brought into contact with the switch SW1, whereby the connector terminals 481a and 481b are short-circuited. On the other hand, connector terminals 463b and 464b are separated from the switch SW2, whereby

the connector terminals 463b and 464b are opened. It is noted the connector terminals 463b and 464b are in contact with the cartridge terminals 483c and 483d; however, both of the cartridge terminals 483c and 483d are opened, and thus, the connector terminals 463b and 464b are never short-circuited.

Referring to Figure 6 and Figure 7, an OE output port of the high-speed processor 52 is connected to OE input ports of the internal ROM 56 and the external ROM 58 (at the time the cartridge is attached). A CE1 output port of the high-speed processor 52 is connected to the connector terminal 463b and a CE input port of the external ROM 58 (at the time the cartridge is attached). A CE2 output port of the high-speed processor 52 is connected to the connector terminal 461b. On the other hand, a CE input port of the internal ROM 56 is connected to the connector terminals 462b and 464b. In addition, the system bus 54 includes an address bus 54a and a data bus 54b through which the high-speed processor 52, the internal ROM 56 and the external ROM 58 are connected with each other.

The high-speed processor 52 outputs a chip enable signal 1 or a chip enable signal 2 from the CE1 output port or the CE2 output port, an address signal through the address bus 54a, and an output enable signal from the OE output port. Respective internal ROM 56 and the external ROM 58, when inputting the chip enable signal 1 or the chip enable signal 2 from the CE input port, identify themselves as being selected to be an access destination, and output a data signal in response to the address signal and the output enable signal inputted at the appropriately same time as the time that chip enable signal is inputted. The data signal is applied to the high-speed processor 52 through the data bus 54b.

The chip enable signal 1 and the chip enable signal 2 are outputted in correspondence to different address value. That is, referring to Figure 8, when an address

value of upper 8 bits indicates any of "00" - "3F" and an address value of lower 16 bits indicates any of "FFFF" - "8000" or when an address value of upper 8 bits indicates any of "80" - "BF", the chip enable signal 1 is outputted. On the other hand, when an address value of upper 8 bits indicates any of "60" - "7F" and an address value of lower 16 bits indicates any of "FFFF" - "8000" or when an address value of upper 8 bits indicates any of "E0" - "FF", the chip enable signal 2 is outputted.

When the memory cartridge 48 is not attached or inserted, the connector terminals 463b and 464b are in a short-circuited state by the switch SW2, and the connector terminals 461b and 462b are in an opened state. Thereupon, the chip enable signal 1 is inputted to the CE input port of the internal ROM 56, and the chip enable signal 2 is not inputted into any input port. Since the high-speed processor 52 outputs the chip enable signal 1 and the chip enable signal 2 according to the above-described manner, the warning message display program 56a, the karaoke video data 56b, and the karaoke music data 56c (referred to Figure3) read out of the internal ROM 56 are mapped as shown in Figure 9.

The warning message display program 56a is mapped to an address space that the upper 8 bits indicate "00" - "1F" and the lower 16 bits indicate "FFFF" - "8000", and all the warning message display program 56a, the karaoke video data 56b, and the karaoke music data 56c are mapped to an address space that the upper 8 bits indicate "80" - "9F" and the lower 16 bits indicate "FFFF" - "0000". Since high-speed processor 52 starts to access from the upper 8 bits' address of "00", when the power is turned on in a state that the memory cartridge 48 is not attached or inserted, the warning message display program 56a is first executed.

When the memory cartridge 48 is attached or inserted, the connector terminals 463b and 464b are in the opened state and the connector terminals 461b and 462b are in